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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,414	ABEDIFARD, EBRAHIM	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-21* is/are allowed.

6)☒ Claim(s) *1-9,12,14-17 and 22* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0304.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 03/08/2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claims 14-15 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 10-11. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 16-17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: first conductivity material and second conductivity material are not defined in claim 9.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Chien (U.S. Patent No. 6,137,730).

Regarding claim 1, Chien discloses a memory device (Figure 4) comprising: a plurality of memory array blocks (ARRAY BLOCK), each comprising a plurality of memory cells arranged in rows that are coupled together by wordlines (209, ABSTRACT); and a row decoder (RD 208) coupled to the plurality of memory array blocks through the wordlines (Figure 4) , and further including a plurality of external address signals coupled to the row decoder such that a wordline is selected in response to the address signals (Column 1, lines 37-44) , and further including a plurality of sense amplifiers (236) coupled to outputs of the memory cells to detect data in the memory

cells (column 1, lines 34-58), and wherein each memory array block comprises 256 wordlines (ABSTRACT).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi et al. (U.S. Patent No. 6,714,451).

Regarding claims 1-8 , Ooishi et al. disclose a memory device (Figure 1) comprising: a plurality of memory array blocks (BLOCK0-n), each comprising a plurality of memory cells arranged in rows that are coupled together by wordlines (Figure 2, WL); and a row decoder (20) coupled to the plurality of memory array blocks through the wordlines (Figure 1) , and further including a plurality of external address signals (801) coupled to the row decoder such that a wordline is selected in response to the address signals (Figure 1) , and further including a plurality of sense amplifiers (Column 14, lines 6-11) coupled to outputs of the memory cells to detect data in the memory cells, and wherein each memory array block comprises 256 wordlines (Figure 1), and wherein the

plurality of memory cells are flash memory cells (Column 1, lines 11-16), and wherein the memory device is a NAND flash memory device, and wherein the memory device is a NOR flash memory device (Column 1 ,lines 10-42).

Regarding claims 9, 13, Ooishi et al. disclose a flash memory device comprising (Figure 1) : a plurality of n-wells comprising an n-type conductivity material, a plurality of p-wells comprising a p-type conductivity material, each p-well located within an n-well (Figure 3) ; a plurality of flash memory array blocks (Figure 1) , each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines, each flash memory array block located within a different p-well of the plurality of p-wells; and a row decoder (Figure 1, 20) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals (Figure1).

Regarding claim 12, Ooishi et al. disclose a memory device (Figure 1) comprising: a plurality of memory array blocks (MEMORY CELL ARRAY BLOCK) arranged in rows comprising at least two memory array blocks, each memory array block comprising a plurality of memory cells arranged in rows that are coupled together by wordlines; and a plurality of row decoders, each row decoder coupled to a subset of the plurality of memory array blocks through the wordlines (Figure 1).

Regarding claim 22, Ooishi et al. discloses an electronic system comprising: a processor (Figure 1, 17) that controls operation of the electronic system and generates address signals; and a flash memory device (MEMORY CELL ARRAY BLOCK) coupled to the processor, the device comprising a plurality of memory array blocks (MEMORY

CELL ARRAY BLOCK)), each comprising a plurality of memory cells arranged in rows that are coupled together by wordlines (Figure2); and a row decoder (Figure 1, 20)coupled to the plurality of memory array blocks through the wordlines, the row decoder coupled to the address signals and selecting a wordline in response to the address signals (Figure 1).

Allowable Subject Matter

11. Claims 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-11 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Chien (U.S. Patent No. 6,137,730), Ooishi et al. (U.S. Patent No. 6714,451) and others, does not teach the claimed invention having a voltage of 0V is applied to the n-well and a voltage of –5V is applied to the p-well of an unselected flash memory array block during an erase operation, and The tlash memory device of claim 9 wherein a voltage of 5V is applied to the n- well and a voltage of 5V is applied to the p-well of an unselected flash memory array block during a program operation.

12. Claims 18-21 are allowed.

Claims 18-21 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Chien (U.S. Patent No. 6,137,730), Ooishi et al. (U.S. Patent No.

6714,451) and others, does not teach the claimed invention having a method for programming and erasing a memory cell as claims 18-21 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER